We Claim:

1. A method for fabricating a MOSFET with a gate channel of a predetermined, very small channel length, the method which comprises the following steps:

producing a dielectric on a semiconductor substrate;

applying a first gate layer to the dielectric, the first gate layer comprising polysilicon;

forming an intermediate layer, to serve as a diffusion barrier, on the first gate layer;

applying a second gate layer, the second gate layer comprising tungsten;

masking the second gate layer to define a width of the second gate layer to be greater than the predetermined channel length;

anisotropically etching the second gate layer, the intermediate layer, and the first gate layer;

isotropically laterally undercutting the first gate layer under the second gate layer selectively with respect to the dielectric, with respect to the intermediate layer, and with respect to the second gate layer, thereby utilizing an etching gas containing hydrogen bromide in a dry etching process, and

controlling the etching process for forming the first gate layer with a predetermined width less than the width of the second gate layer and corresponding to the predetermined channel length.

2. The method according to claim 1, which comprises forming the diffusion barrier of tungsten nitride.

3. The method according to claim 1, which comprises controlling the width of the first gate layer by a width of the second gate layer and by a duration of the lateral undercutting of the first gate layer under the second gate layer.

4. The method according to claim 1, which comprises controlling a width of the first gate layer during the undercutting step by controlling a concentration of an etchant.

5. The method according to claim 1, wherein the predetermined width of the first gate layer is equal to the predetermined channel length.

6. The method according to claim 1, which comprises continuing the anisotropic etching of the second and first gate layers until the dielectric is reached.

7. The method according to claim 1, which comprises undercutting with an isotropic plasma etching step.

8. The method according to claim 1, wherein the width of the second gate layer is between 120 and 300 nm.

9. The method according to claim 1, wherein the width of the first gate layer is between 30 and 150 nm.

10. The method according to claim 1, wherein the gate dielectric comprises silicon dioxide.

11. The method according to claim 1, which comprises forming the second gate layer with a higher electrical conductivity than the first gate layer.

12. The method according to claim 1, which comprises introducing source/drain implantations and diffusing the implantations under the predetermined width of the second gate layer as far as an edge of the first gate layer.

13. The method according to claim 1, wherein the step of forming the intermediate layer encompasses subsequent silicidation.